Heterogeneous Interconnect Stitching Technology With Compressible MicroInterconnects for Dense Multi-Die Integration

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***Abstract*— In this letter, a heterogeneous interconnect stitching technology is proposed. Stitch chips with high-density fine pitch wires are placed between the substrate and the active chips. Fine-pitch microbumps are used to bond the chips and provide high density and low-energy signaling. Compressible microinterconnects (CMIs) are used to compensate for package non-planarity and enable chip-package interconnection. A testbed with two passive chips and one stitch chip was fabricated and assembled. The post-assembly electrical resistance values of the microbumps and CMIs, as well as the mechanical compliance of the CMIs, are measured. The resistance of the microbumps ranges from 77.8 to 188.3 $\mu\Omega$ and the resistance of the CMIs ranges from 141.2 to 252.9 mΩ. The mechanical compliance of the CMI is approximately 13.7 mm/N with a vertical elastic deformation of up to 30 μm.**

***Index Terms*— 3D IC, flexible interconnects, heterogeneous integration, interconnect, system-in-package.**

I. Introduction

THERE is an ever increasing need to integrate multiple dice of various functionalities, including ASICs, CPUs, GPUs, FPGAs, microsensors, photonics, MEMS, and RF components into a single package [1] [2]. This need has spurred significant research in heterogeneous interconnection platforms, including silicon interposer (2.5D IC [3]), embedded multi-die interconnect bridge (EMIB) technology [4], and chip stacking (3D IC [5]–[7]). While each of the aforementioned solutions has benefits, they also have potential limitations, as noted in Table. I.

To avoid these shortcomings, we present a heterogeneous interconnect stitching technology (HIST) platform to enable the interconnection of multiple dice (or "chiplets") of various functionalities in a manner that mimics monolithic-like performance, yet utilizes advanced off-chip interconnects and packaging to provide flexibility in IC fabrication and design, improved scalability, reduced development time, and reduced cost. Figure 1 illustrates the schematic of a HIST platform. A stitch chip with high-density fine pitch wires is placed between the substrate and the chiplets. Fine-pitch microbumps are used to bond chiplets to the stitch chip to provide high-bandwidth density and low-energy signaling. Compressible microinterconnects (CMIs) are used to compensate for package non-planarity and enable chiplet-package interconnection. CMIs are pressure-contact based interconnects designed to interface with a pad on the package substrate. Compared to competitive solutions, the advantages of HIST include the following: HIST achieves a similar signal bandwidth density as the silicon interposer technology [8], but is not reticle-size limited, thus making it very scalable in size; HIST eliminates the need for through-silicon-vias (TSVs) in the substrate for decreased cost and improved signaling [9]; HIST is based on die-to-die face-to-face bonding, and thus there are no intermediate package levels, which enables higher signal I/O pitch and lower capacitance; and lastly, HIST can be applied to any packaging substrate (organic, ceramic, etc) since HIST is augmented to the top-most surface of the package substrate. The presence of CMIs can also improve system mechanical reliability. In addition, the integration of silicon photonics is another promising application of HIST, as illustrated in Fig. 1.

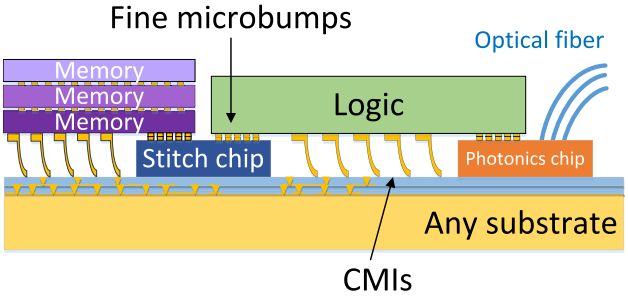

Fig. 1. Schematic of the HIST platform.

II. Fabrication and Assembly

Scanning electron microscope (SEM) images of a chiplet are shown in Fig. 2. In this effort, 20 μm and 10 μm pitch Cu-Au microbumps are fabricated with a lift-off process. The gold-coated NiW alloy CMIs are approximately 55 μm in

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TABLE I
COMPARISON OF DENSE FINE PITCH INTERCONNECT SOLUTIONS

	HIST (THIS WORK)	EMIB [4]	Silicon Interposer [7]	Chip Stacking [6] [7]
Microbump pitch	< 20 µm	~50 µm	30-60 µm	> 7.6 µm
Footprint	Scalable	Scalable	Limited	Scalable (vertical)
Interface	Si-Si Face-to-face	Si-Organic-Si	Si-Si	Si-Si
Require TSV	No	No	Yes	Yes
Agnostic to substrate	Yes	No	-	-

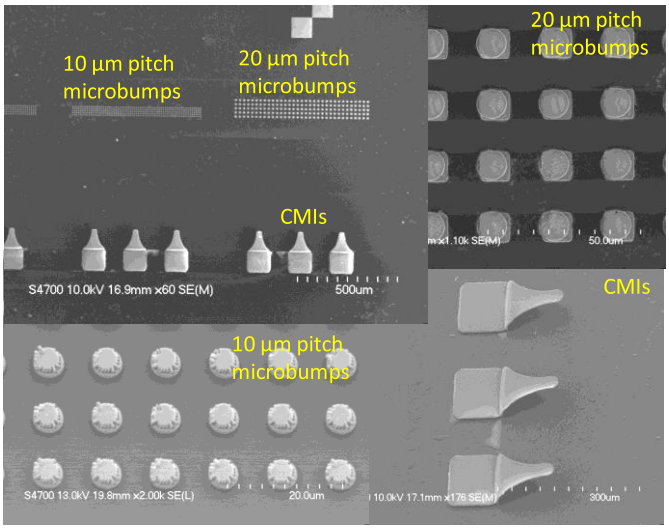

Fig. 2. SEM images of the chiplet with microbumps and CMIs.

height, 20 μm in width at the tip, 200 μm in length, and are on a 200 μm pitch. Since CMIs are lithographically defined, they can be miniaturized. In order to maximize the vertical elastic range of motion, an approximately tapered design is adopted to distribute the stress along the body of the CMI during deflection. The upward-curved profile of the CMI ensures that the tip of the CMI remains in contact with the mating pad during deflection.

The chiplets were assembled with a Finetech Fineplacer Lambda flip-chip bonder using a thermal compression process. A force of 5 N was applied during bonding with a maximum temperature of 300° C. Optical and x-ray images of the assembled chiplets are shown in Fig. 3. In this demonstration, the stitch chip on the package was emulated by a step-like structure that is approximately 40 μm in height. As shown in the SEM image, part of the chiplet is bonded to the stitch chip, while the rest of the chiplet is suspended above the substrate and supported by the CMIs. Note that the CMIs traverse the height of the stitch chip that is "sandwiched" between the package substrate and the chiplets to provide the needed electrical interconnection to the package substrate (power delivery and other signaling needs). Figure 3 shows a die micrograph and an X-ray image of the assembled HIST testbed. Two chiplets are placed side-by-side on the stitch chip and the substrate. For testing purposes, approximately half of the chiplet area is occupied by microbumps to support high density interconnects to the stitch chip, while the other half is occupied by CMIs that interconnect to the package substrate. In this testbed, the dice are not underfilled. However, technologies for applying underfill within the small

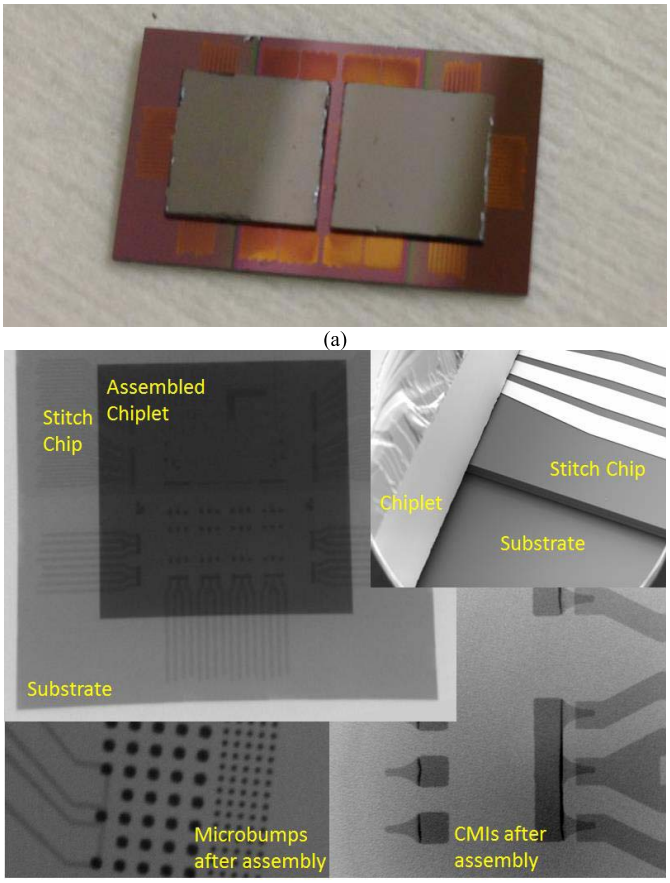

Fig. 3. (a) Optical image; (b) X-ray and SEM images of the HIST testbed after assembly.

gap and the high-density microbumps have been demonstrated in [10] and may be used when needed.

III. MECHANICAL AND ELECTRICAL MEASUREMENTS

Mechanical compliance is a key property of the CMI and was measured using a Hysistron Triboindenter, as shown in Fig. 4. Five CMIs located at different regions of the chiplets were measured, and the results are shown in Fig. 4. The indentation results show that the mechanical compliance is approximately 13.7 mm/N, and CMIs can achieve up to 30 μm of vertical elastic deformation.

The post-assembly resistance values of the 20-μm pitch microbumps and the CMIs are measured with Kelvin resistance structures. A Keithley 2182A voltmeter and a Keithley 6220 current source are used to perform the measurements with a Karl-Suss probe station, as shown in Fig. 5. The resistance of the microbumps ranges from 77.8 $\mu\Omega$ to 188.3 $\mu\Omega$.

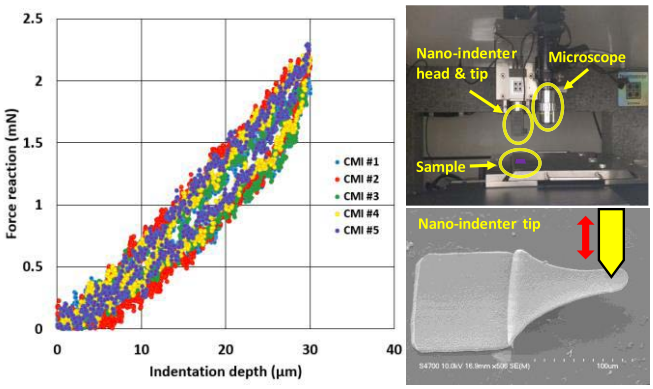

Fig. 4. CMI indentation test setup and results.

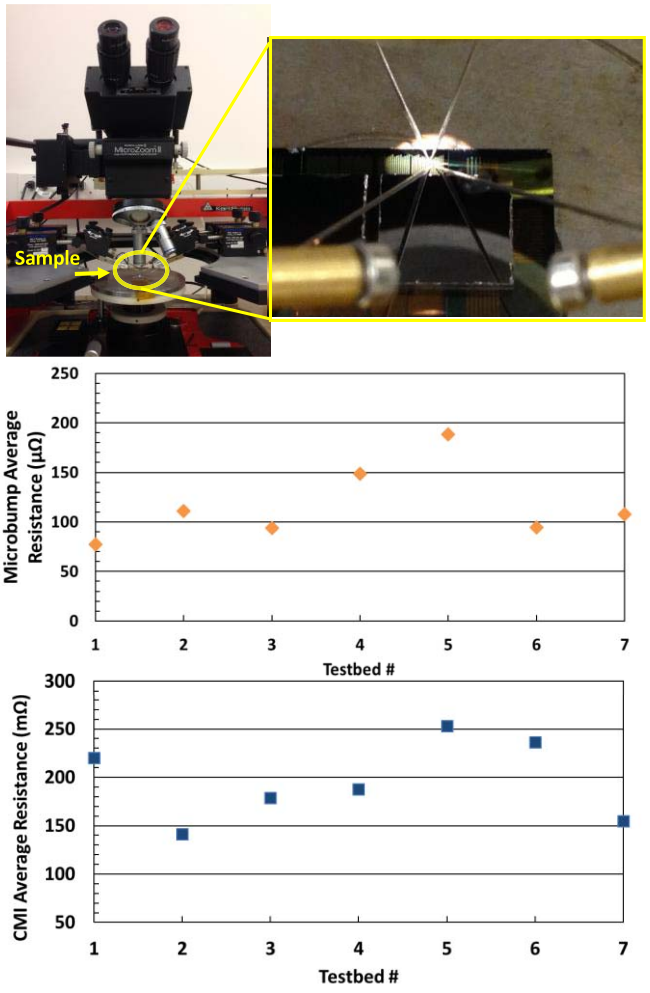

Fig. 5. Kelvin resistance measurement setup and results.

The cause of the data variation is the misalignment of the assembled testbeds due to limits of our in-house flip-chip bonder. The resistance of the CMIs (including contact resistance) ranges from 141.2 mΩ to 252.9 mΩ. The current carrying capability of flexible interconnects of similar materials and approximate dimensions has been demonstrated to be up to 1 A [11]. Simulations using ANSYS HFSS show that the insertion loss of the CMIs is approximately 0.26 dB at 20 GHz. This value is significantly lower than the loss of TSVs [3], [12]. The inductance (extracted from the simulated S-parameters at 1 GHz) of the CMIs is approximately 156 pH. The size of the CMIs can be decreased since they are lithographically-defined, which will further decrease the loss and inductance.

IV. Conclusion

In this letter, a Heterogeneous Interconnect Stitching Technology (HIST) testbed is fabricated and assembled for the first time. The post-assembly electrical resistance values of the microbumps and compressible microinterconnects are measured. The proposed HIST platform strives to achieve monolithic-like performance, yet utilizes TSV-less high-density interconnection using stitch chips that are integrated between the chiplets (i.e., logic-, memory-, sensors-die, etc) and the package substrate.

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